



Application No. 10/626,620

Amendment dated October 30, 2006

After Final Office Action of September 6, 2006

Docket No.: M4065.0567/P567-A

REMARKS

Claims 62-65 are withdrawn. Claims 9-13 and 62-65 are pending in the present application.

Claims 9-13 stand rejected under 35 U.S.C. § 102(a) as being anticipated by Admitted Prior Art ("APA"). Applicant respectfully traverses this rejection.

Claim 9 recites a memory device comprising "a gate stack pair with a space between them defining a contact opening" and "a vertical oxide spacer adjacent to each gate stack of said gate stack pair." Claim 9 further recites "a nitride layer adjacent each said vertical oxide spacer and each said gate stack, . . . wherein said vertical oxide spacer is *recessed from a top surface of each gate stack.*" Emphasis added. The APA does not disclose all the limitations of claim 9.

The APA discloses "a pair of typical flash cell gate stacks 1 positioned adjacent to each other on a substrate 2." Paragraph [0006]; FIG. 1. The APA discloses that each stack "includes a tunnel oxide layer 3," a "polysilicon floating gate 4 is positioned on top of the tunnel oxide layer 3 and an oxide/nitride/oxide (ONO) layer 5 is positioned on top of floating gate 4." Id. The APA also discloses "a polysilicon control gate 6 is typically formed on top of the ONO layer 5 with a tungsten silicide layer 7 formed on top of the control gate 6" and a "cap 8, which is . . . positioned on the tungsten silicide layer 7." Id. Hence, according to the disclosed APA, the gate stack comprises layers 3 through 8, with the top surface of cap 8 being the top surface of the gate stack.

The APA further discloses that the gate stacks have "oxide seams (spacers) 11 separating nitride spacers 13 from gate stack 1." Paragraph [0007]; FIG. 2C. As can be seen in FIGs. 2A-3, the vertical oxide spacers 11 have a top end that is level with the top

surface of each gate stack. Thus, the vertical oxide spacers 11 of the APA are at the same level as the top surface of each gate stack and not "recessed from a top surface of each gate stack," as recited in claim 9.

Since the APA does not disclose all the limitations of claim 9, claim 9 and claims 10-13 depending therefrom are patentable over the prior art. Accordingly, Applicant respectfully requests that the 35 U.S.C. § 102(a) rejection of claims 9-13 be withdrawn.

In view of the above amendment, Applicant believes the pending application is in condition for allowance.

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Respectfully Submitted,

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